GaAs Heterojunction Bipolar Transistor Device and IC Technology for High-Performance Analog and Microwave Applications

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Abstract—**This paper discusses the GaAs/AlGaAs N-p-n heterojunction bipolar transistor (GaAs HBT) technology and its application to analog and microwave functions for high-performance military and commercial systems. In focused applications the GaAs HBT offers key advantages over alternative advanced silicon bipolar and III–V compound field-effect transistor (FET) approaches. The TRW GaAs HBT device and IC fabrication process, basic HBT dc and RF performance, examples of applications, and qualification work are presented and serve as a basis for addressing general technology issues. A relaxed 3 μm emitter-up, self-aligned HBT IC process permits a combination of excellent transistor dc and RF performance including simultaneous $f_T, f_{max} \approx$ 20–40 GHz and dc current gain $\beta \approx$ 50–100 at useful collector current densities $J_C \approx$ 3–10 kA/cm^2, Early voltage $V_A \approx$ 500–1000 V, and MSI–LSI integration levels. These capabilities facilitate versatile dc–20 GHz analog/microwave as well as 3–6 Gbit/s digital, 2–3 Gs/s A/D conversion, and monolithically combined functions—with producibility. In analog and microwave applications, key improvements are realized over Si bipolar and GaAs-related FET (such as MESFET and HEMT) approaches in combinations of operational frequency, power consumption, gain–bandwidth product, harmonic distortion, and phase ($1/f$) noise.**

I. INTRODUCTION

THE GaAs/AlGaAs heterojunction bipolar transistor (GaAs HBT) is emerging as a versatile device technology attractive for application to high-performance military as well as commercial systems, including communication (microwave, optical), electronic warfare, radar, smart weapon, and instrumentation. It has the potential to provide a more efficient solution to front-end signal processing requirements through intrinsic device advantages [1], [2] than the most competitive silicon bipolar transistor [3], [4] and III–V compound field-effect transistor (FET, such as MESFET and HEMT) technologies [5], [6], as summarized in Fig. 1. Applications include analog/microwave [2], [7]–[13], digital [14], and analog/digital (A/D) conversion functions [15], [16] previously limited to GaAs-related FET and Si device technologies. The GaAs HBT offers significant improvements in combinations of operational frequency, power consumption, gain–bandwidth product, harmonic distortion, $1/f$ noise, radiation hardness, and size reduction—with cost effectiveness.

Compared to other HBT technologies such as those based on Si/SiGe [17] and InP/In(Al, Ga)As [18] heterojunctions, the GaAs HBT is more mature. With key demonstrated capabilities and significant growth potential, the GaAs HBT is establishing a niche for itself in front-end signal processing applications over the most competitive GaAs MESFET/HEMT and advanced Si homojunction bipolar transistors such as the super self-aligned technology (SST) [3]. The highest performance bipolar implementation for the GaAs HBT is the N-p-n transistor (N denoting wider band gap than n and p) operating in nonsaturating circuit topologies such as the emitter-coupled logic (ECL) type as opposed to the slower saturating integrated-injection logic (I^2L). A GaAs N-p-n HBT I^2L termed heterojunction inverted transistor integrated logic (HI^2L) (19) has been used to achieve LSI–VLSI capabilities. This is facilitated by the inherently high packing density of the HI^2L logic, which has emitter-down HBT'sconnected via a common n^+ substrate and collectors which are simple Schottky metal contacts at the surface. Despite the GaAs HBT HI^2L's relatively low speed (100–200 MHz clock) and high power consumption, its radiation hardness makes the technology appealing. On the other hand the higher performance ECL-type HBT device and circuit approaches require more complex emitter-up structures and are currently in the 1–5 K transistor integration levels [14], [15]. Discrete GaAs P-n-p HBT's are attractive due to the lower resistance base, but the disadvantages are higher hole base-transit time and higher emitter and collector resistances. Useful performance has been demonstrated [20]; however its utility lies in monolithic

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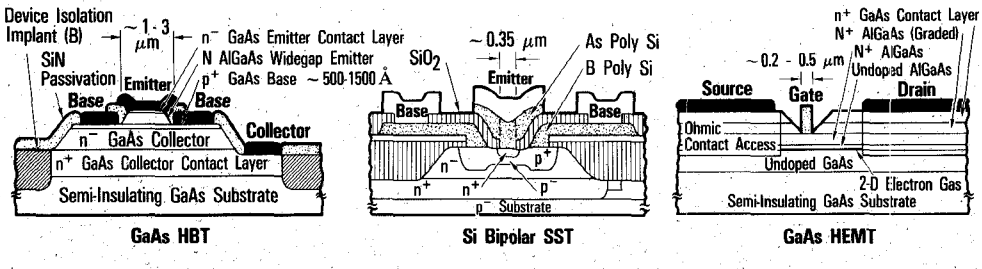


Intrinsic Device Characteristics	GaAs HBT	Si Bipolar SST	GaAs HEMT/MESFET
• Device Speed (f_t, f_{max})	~50-200 GHz; ~1-3 μm Emitter	~20-40 GHz, ~0.35 μm	~0.2-0.5 μm Gate
• Current/Effective Chip Area	~50 kA/cm^2	~2-5X Lower	~5-10X Lower
• Device Matching	V_{be} ~ 1-2 mV	Comparable	~3-5X Worse
• Transconductance (g_m)	~5-10 K mS/mm	Comparable	~20-100X Lower
• Output Conductance (g_o)	~0.2 mS/mm	~10-20X Higher	~25-100X Higher
• Trapping Effects	1/f Corner < 1 MHz	Comparable	~10-100X Higher
• Input Impedance	Base Input Current	Same	Voltage-Controlled Gate
• White Noise (10-20 GHz)	~4-6 dB	Comparable	~2-7X Lower
• Radiation Hardness	>500 Mrad; >1x10^{14} Neutrons/cm^2	20-50X Lower	Comparable
• Substrate Capacitance	No	Yes	No
• Power Consumption	High	High	Medium
• Integration Level	MSI - LSI	LSI - VLSI	LSI

Fig. 1. Comparison of GaAs HBT with GaAs MESFET/HEMT and Si bipolar super self-aligned technology (SST) type transistors.

integration with N-p-n HBT's for complementary functions such as in active loads, current sources, and push–pull amplifiers. High-performance complementary N-p-n/P-n-p HBT integration will be difficult to achieve due to complex material processing requirements.

The GaAs N-p-n HBT designed for nonsaturating (ECL type) applications is compared here to the GaAs FET and Si bipolar SST-type technologies, considered to be the most competitive approaches. Key advantages presented in Fig. 1, which provide the motivation for the technology development, are further examined here.

A. GaAs HBT Versus MESFET and HEMT

Compared to the MESFET and HEMT, the GaAs HBT as a vertical bipolar device is not particularly suited for low-white-noise applications or convenient planar processing, but it has many advantages:

- The HBT speed is governed largely by the transit time through thin vertical layers (base/collector several thousand angstroms thick) easily realized by epitaxial growth, which results in microwave/millimeter-wave frequency capabilities (f_T, $f_{max} \approx$ 100–200 GHz) with relaxed 1–3 μm lithographic (optical) dimensions [2], [7]–[10]. The MESFET/HEMT speed is controlled by a lateral transit time determined by a lithographically defined gate. To achieve similar frequencies the gate dimensions are typically 0.2 to 0.5 μm [5], [6], requiring complex electron-beam lithography.
- The HBT's higher transconductance g_m (10–100 times, depending on the output current) results from the bipolar's exponential output current–input voltage variation compared to the FET's quadratic or linear characteristic resulting from indirect modulation of charge carriers through a depletion or intervening layer between the gate and the active channel. The high g_m permits small input voltage swings and facilitates low (common-collector) output impedance for fast charging of load capacitances in IC's [14], [15]. The HBT's exponential I–V characteristic also facilitates efficient nonlinear functions such as limiting and logarithmic amplifiers [11], [12] and multiplier/mixers.
- The lower (common-emitter) output conductance g_o of the HBT results from the highly doped base, which minimizes base width modulation and the variation of the collector current with the collector–emitter voltage. In an analogous FET drain current/voltage behavior the g_o is governed by surface and active channel–substrate leakage and trapping effects, leading to frequency-dependent characteristics undesirable for high-accuracy analog applications. The HBT's low g_o yields the high device linearity and dc voltage gain important in analog applications [2], [7], [16].
- The HBT's better device matching results from the dependence of the turn-on voltage V_{BE} on the intrinsic material energy gap (which is easily controlled during the epitaxial growth). This is to be compared to the MESFET and HEMT pinch-off voltage V_P, which depends directly on the doping and thickness of the active channel. The result is highly matched differential pairs for high-accuracy comparators (A/D converters) [15] and low offset dc coupling (analog amplifiers) [11]–[13] and input voltage

matching for low voltage swings (high-speed, low-power IC's) [14], [15].

- The HBT's reduced trapping effects and lower $1/f$ noise result from carrier flow primarily through active junctions isolated from surfaces and substrate interfaces. In FET's, the carriers travel between surface and active channel–substrate interfaces, experiencing greater trapping effects. The benefit is in circuits such as mixers, oscillators, and dividers where the baseband $1/f$ noise gives rise to phase noise at the RF output [7], [9].
- The HBT's higher current per effective transistor area than the GaAs MESFET or HEMT arises from the vertical structure of the HBT compared to the lateral structure for FET's. The entire emitter area contributes to the current rather than a thin channel as in FET's. The result is a higher current (power) handling capability per effective transistor area. In addition the HBT permits breakdown voltages to be easily tailored for optimized power performance (class B and C amplifiers) via epitaxial growth control of the collector doping and thickness [8], [10].
- Greater radiation hardness in dose rate environments [21] results from the shielding of the active junctions from the semi-insulating substrate by the highly doped n^+ subcollector, leading to freedom from long-term transients (trapping effects) to which MESFET's are particularly susceptible.

B. GaAs HBT Versus Advanced Homojunction Silicon Bipolar (SST Type)

Compared to the advancing Si-based high-speed LSI–VLSI bipolar technologies such as the SST, the GaAs HBT is presently limited in integration complexity to MSI–LSI levels. The Si bipolar SST-type technology has demonstrated increasing speed performance ($f_T > 20$ GHz), which also makes it attractive for analog/microwave type functions. However this performance is at the expense of ≈ 0.35 μm emitter dimensions and relatively complicated processing [3]. The GaAs HBT with heterojunction emitter, higher mobility material, and semi-insulating substrate offers many advantages:

- The HBT's higher gain–bandwidth product with relaxed geometries arises from the higher mobility and the heterojunction emitter which permits the optimization of the emitter and base doping for reduced parasitics [1]. Higher performance analog/microwave as well as digital and A/D circuits with simplified 1–3 μm optical lithographic processing result [2], [7]–[16].
- The higher output impedance (Early voltage) results from the high base doping permitted by the heterojunction, which minimizes the base width modulation. Higher accuracy and lower harmonic distortion performance result [7].
- The semi-insulating substrate permits simpler processing (device isolation) and higher circuit speeds through lower parasitic substrate capacitance and lower loss matching networks for MMIC applications [2], [7]–[16].
- The HBT's greater radiation hardness arises from the shielding of the active junctions from the semi-insulating substrate by the highly doped n^+ subcollector layer, the fact that there are no stray p-n isolation junction effects (latchup), high base doping, and Fermi-level pinning at the surface [21].

C. GaAs HBT Technology Application Impact

The high performance potential of the GaAs HBT has generated extensive investigations over the past ten years by academic and industrial laboratories. Most of the work has been stimulated by the HBT's high-frequency capabilities, exemplified by its higher circuit speeds (toggle rate) and lower delay–power product with relaxed lithographic geometries compared to the most competitive III–V FET and Si bipolar device technologies. Other inherent GaAs HBT advantages such as low harmonic distortion, exponential current output/voltage input transfer function, low $1/f$ noise, and high-efficiency output power capabilities are receiving increasing attention. However, until recently there has been little convergence toward real system insertion. The drive towards technology maturation has been motivated by the prospects for significantly improving military (TRW) as well as commercial electronic systems. The intrinsic advantages of the GaAs HBT over GaAs MESFET/HEMT and SST-type Si bipolar are somewhat offset in real system applications by the greater maturity of these other technologies.

While the GaAs HBT's advantages are attractive for broad circuit functions, advances in the more mature competing technologies will require careful application selection for the HBT. The GaAs HEMT is ideal for ultra-low-white-noise requirements and the GaAs MESFET for generic microwave functions, while the Si bipolar and CMOS are best suited for complex VHSIC-type signal processing functions requiring LSI–VLSI integration levels. The GaAs HBT will be attractive for niche functions that require combinations of high speed, low distortion, high dynamic range, and low phase noise with producibility. Key functions that the GaAs HBT is expected to impact, with many of these already demonstrated and others in development (particularly at TRW), are as follows:

1) Analog and Microwave/Millimeter-Wave Functions: The HBT's high f_T and f_{max} along with other inherent device advantages make it ideal for front-end functions from dc to microwave/millimeter-wave frequencies:

- The high linearity associated with its low output conductance g_o is attractive for low-harmonic-distortion applications [7] such as an output stage amplifier following a MESFET or HEMT low-noise input

amplifier. A hybrid balanced amplifier with ≈ 33 dBm third-order intermodulation intercept point (IP3) over 7–11 GHz has been developed at TRW with 2–3 times the IP3/dc power ratio of MESFET approaches (Section IV); monolithic microwave IC (MMIC) versions are in progress.

- The high g_m at low collector current makes possible very low power dissipation microwave amplifiers. A hybrid distributed amplifier with flat 10 dB gain from dc to 9 GHz dissipating 75 mW has been developed at TRW (Section IV); MMIC versions are in progress.
- The high intrinsic gain (g_m/g_o) combined with high speed and freedom from trapping effects makes it ideal for wide-band analog/microwave amplifiers. Fixed gain dc to >10 GHz feedback and distributed amplifiers have been developed at TRW (Section IV).
- The high current density and high breakdown voltage are attractive for high-efficiency class B and class C power applications such as transmitters for phased-array radar. Rockwell [8] and Texas Instruments [10] have demonstrated *X*-band power amplifiers with 2–4 W output per mm of emitter length with 40–50 percent power-added efficiencies. The push is now toward millimeter-wave frequencies. Rockwell has demonstrated 1.7 W per mm of emitter length at 59 GHz (2.5 dB gain) [8]. However, for practical high output powers much work is needed in establishing reliable structures.
- The high-frequency performance combined with exponential output current–input voltage relation and high substrate isolation makes it attractive for monolithic logarithmic IF amplifiers (compression of wide dynamic range signals) and analog multiplier/mixers in active development at TRW (Section IV). New monolithic log amplifier capabilities are being achieved with GaAs HBT's [11], [12]. Multiplier/mixers based on Si bipolar Gilbert-cell designs have been developed with higher bandwidths and lower spurs.
- The low $1/f$ noise (<1 MHz noise corner) is attractive for low-phase-noise oscillators and dividers in frequency synthesizer applications. The GaAs HBT is extending the bipolar capabilities to microwave/millimeter-wave frequencies. Oscillators demonstrated include 20–28 GHz fundamental (NEC [9]) and 25–32 GHz push–push (TRW [7]) (Section IV) designs while static 1/4 dividers have achieved impressive operation beyond 26 GHz (Rockwell [8]).

2) Monolithically Combined Microwave/Digital Functions: Monolithic integration involving combinations of analog/microwave, digital, and A/D conversion functions is attractive for system simplification. For III–V FET's such single-chip multifunctions are more difficult because of the need to control two threshold voltages: low pinch-off for digital and A/D devices and high pinch-off/recessed channel for microwave devices. Si bipolar is limited in microwave performance. On the other hand the GaAs HBT is ideal for combined microwave/digital functions since the same epitaxial structure facilitates microwave and digital performance:

- Simultaneous analog and digital functions, operating in the 1–3 GHz regime, are already present in A/D conversion circuits [15], [16].
- Combined microwave/digital functions have been demonstrated with the TRW HBT process through a dc–6 GHz amplifier/digital divider designed for low input signals (−10 to −25 dBm) and a 5-bit digitally controlled switched gain/attenuator [13] (Section IV).
- Complex multifunctions could include combinations of RF mixers, linear/nonlinear amplifiers, and A/D converters with high-speed digital dividers, mux/demux, and logic. The TRW HBT process can simultaneously provide microwave frequencies >20 GHz with useful dc current gains of 50–100 for A/D conversion functions [7]. Rockwell has demonstrated high gain microwave and >26 GHz 1/4 digital dividers on the same wafer. Monolithic integration of VCO's, while attractive, may be limited by specific isolation, spur, and frequency tuning requirements.

The following sections focus on the impact of the GaAs HBT technology on high-performance analog and microwave applications. A maturing TRW GaAs/AlGaAs 3 μm emitter-up N-p-n HBT device and IC technology (currently undergoing technology transfer to a pilot production facility) serve as the discussion vehicle. The device/IC fabrication approach, HBT dc and RF performance, examples of demonstrated functions and current developments, and technology qualification work are presented.

II. HBT Device/IC Fabrication Technology

GaAs HBT fabrication processes are currently being customized at TRW [7], [11]–[13], [15], [16] and similarly by other laboratories [2], [8]–[10], [14], [22]–[25] for various optimized analog, digital, A/D conversion, and microwave/millimeter-wave applications (Fig. 2). The trade-off is in the operational frequency, current gain, and the device/circuit complexity determined by the material parameters and the processing complexity. The latter aims at reducing dimensions and parasitic resistances and capacitances using self-aligned lithography and isolation implant techniques to achieve higher frequencies but at the expense of β degradation and yield. The mesa HBT approach is preferred because planar access techniques which require dopant implantation/activation or diffusions tend to degrade the β via increased carrier recombination and smearing of the emitter heterojunction.

Many important functions can be realized with the relatively simple 3 μm emitter-up, self-aligned base ohmic metal (SABM) mesa HBT IC process, in which the base ohmic metal is self-aligned to the emitter mesa edge to

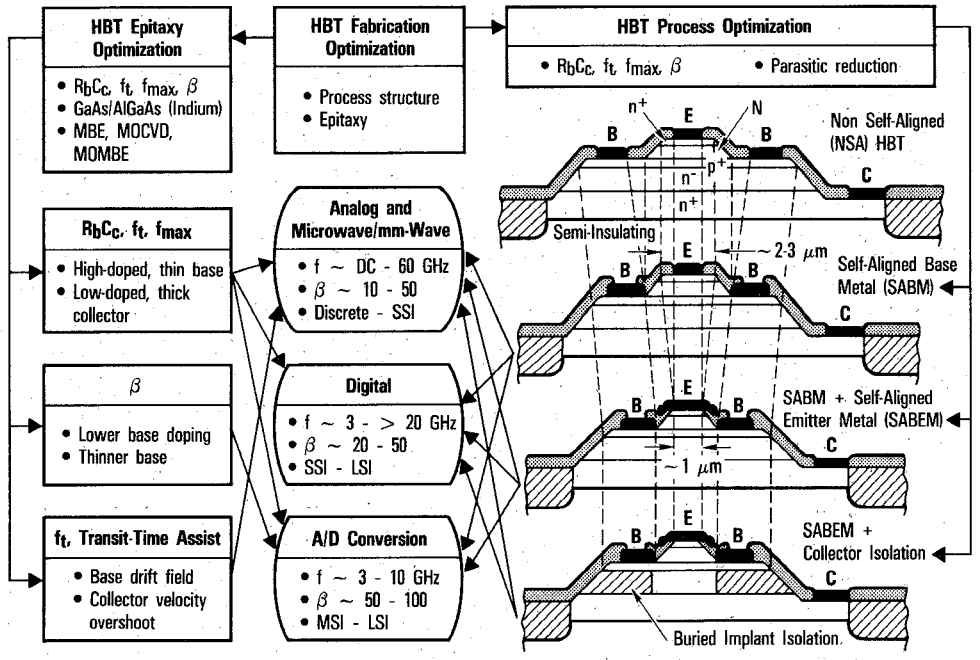


Fig. 2. GaAs HBT fabrication optimization for analog, digital, A/D conversion, and microwave/millimeter-wave applications.

reduce the parasitic external base resistance. Since the emitter ohmic contact is not self-aligned, the free alignment of a typical 1 μm ohmic contact via requires emitter widths of 2–3 μm. The more relaxed 3 μm emitter offers a combination of high performance (dc to $\approx$ 20 GHz and $\beta \approx 50$–100) with producibility (SSI–LSI) for near-term insertion. This HBT device/IC fabrication process was designed for versatile nonsaturating (ECL-type) analog/microwave, digital, and A/D conversion applications with circuit densities up to $\approx$ 5 K transistors. Tighter lithographic control can permit useful yields with 2 μm emitter designed for higher speeds and lower power. The 3 μm emitter SABM HBT IC technology is the focus of this paper.

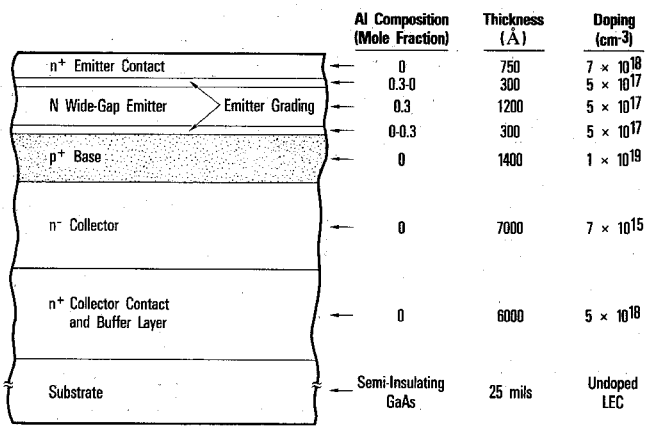
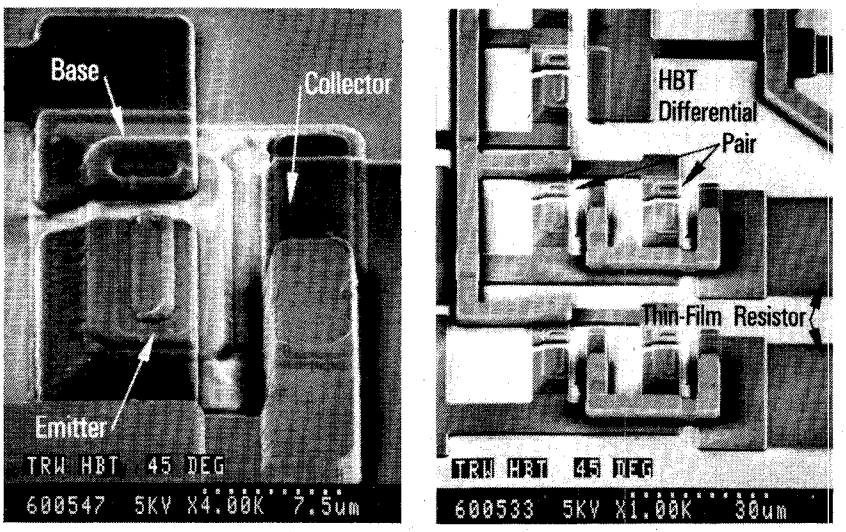


Fig. 3. Versatile GaAs/AlGaAs N-p-n HBT epitaxial growth structure designed for analog/microwave as well as digital and A/D conversion applications.

A. Epitaxy

For near-term system insertion of the HBT technology, MBE epitaxy in general offers an attractive combination of maturity and excellent growth parameter control. These capabilities have led to a variety of material enhancements such as InAs(InGaAs) emitter ohmic contact layers [23], built-in drift fields [23], velocity overshoot structures [22], and double heterojunctions [26] to further improve performance, particularly current gain β and f_T. While the MBE technique affords uniform and repeatable atomic layer growth of GaAs/AlGaAs heterostructures, the dopant control (n-type Si and p-type Be) is of primary concern in the HBT industry; in particular, control of Be diffusion and carry-forward movement from the base into the AlGaAs emitter graded region as the subsequent epitaxial layers are grown will result in a degradation of β via increased hole injection and recombination effect [27]. Alternative epitaxial growth approaches include metal-organic chemical vapor deposition (MOCVD) [11] and metal-organic MBE (MOMBE), which offer the potential for better surface morphology, higher throughput, and lower cost but require further development, particularly p-type base dopant (Zn, C) control.

In this work a simplified GaAs/AlGaAs N-p-n HBT emitter-up, single heterostructure, shown in Fig. 3, is implemented for device and IC fabrication ease. High dc β of 50–100 and $f_T, f_{max} \approx$ 20–40 GHz ($\approx$ 3–10 kA/cm^2) are achieved without complex enhancements. The emitter heterojunctions are graded to maximize electron injection efficiency and hole injection suppression. To reduce the base resistance–collector capacitance (R_BC_C) time constant, the base layer is relatively thick and heavily doped while the collector layer is lightly doped and thick. The relatively thick base and collector layers increase the tran-



(a) (b)

Fig. 4. Scanning electron micrographs showing examples of (a) 3×10 μm^2 self-aligned base ohmic metal (SABM) HBT transistor and (b) integrated circuit portion.

sit time and reduce f_T, but improve the fabrication control using wet chemical etching, reduce the collector capacitance, and increase the breakdown voltage. While the HBT profile can be adjusted to trade off β and f_T, the same profile of Fig. 3 affords versatile analog/microwave, digital, and A/D conversion performance.

B. Device and Integrated Circuit Process

The 3 μm emitter SABM HBT device (Fig. 2) and IC process was designed as an engineering trade-off between useful microwave/digital performance and fabrication ease. This partially self-aligned mesa HBT IC fabrication structure integrates key device components including transistors, Schottky diodes, laser trimmable thin-film resistors (TFR's), and metal–insulator–metal (MIM) capacitors. The usefulness of the baseline 3 μm emitter SABM IC process has been verified from discrete HBT's (as large as quad 3×60 μm^2) to MSI–LSI circuits designed with 3×3 μm^2 emitter HBT's. The HBT self-aligned base ohmic metal (using a double-resist technique) essentially eliminates the parasitic external R_B by minimizing the ohmic metal to emitter spacing (within ≈ 0.15 μm), increasing f_{max} by ≈ 50–80 percent. The width of the surrounding base metal is reduced to ≈ 1.5–2 μm, consistent with the ohmic contact transfer length of ≈ 1 μm and minimal parasitic collector–base area/capacitance. The active device layers are accessed by a combination of selective (emitter mesa) and nonselective wet chemical etches. Ohmic contact resistances are the primary parasitic sources and are minimized by using AuBe/Pd/Au and AuGe/Ni/Ti/Au for p-type and n-type ohmic contacts, respectively. A multiple boron damage implant is used for device isolation, yielding several GΩ/sq. Plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN) is used to passivate the GaAs surface and serves as dielectric insulator for metal–insulator–metal (MIM) capacitors and double-level metal interconnection (Ti/Pt/Au and Ti/Au). Depending on the application, the interconnects follow a 4 μm line/4 μm spacing or 3 μm line/3 μm spacing layout design rule. Air bridge interconnects and thinned substrates for transmission lines and backside vias are also available. Fig. 4 shows scanning electron micrographs of the baseline 3×10 μm^2 HBT and IC portion representative of analog/microwave as well as digital and A/D conversion circuits.

Other key device components integrated with the SABM HBT are a Schottky barrier diode for fast switch applications and laser trimmable thin-film resistors which include nichrome (NiCr) and/or cermet (SiOCr). The Schottky diode is fabricated on the n^- collector layer using Ti/Pt/Au first interconnect metal as the Schottky barrier metal [16] with diode cutoff frequency > 500 GHz. The thin-film resistors can be chosen as nichrome (≈ 100 Ω/sq) and/or cermet (≈ 500 Ω/sq) depending on the application. Laser trimming, cutting for nichrome and annealing for cermet, is performed through the nitride passivation with an underlying SiN protecting the GaAs. This trimming capability is essential in high-accuracy analog applications where transistor/resistor differential pair matching is critical.

III. Basic HBT Device DC and RF Performance

For the 3 μm emitter SABM HBT process various emitter configurations are available in the design library including a 3×3 μm^2 emitter for more complex circuit applications to multiple 3×60 μm^2 emitter HBT's for higher power applications. For the basic fabrication process the HBT β is relatively insensitive to device size (periphery), and f_{max} performance is roughly independent of emitter area (reduced area and junction capacitance is offset by the increased contact resistance). For the purpose

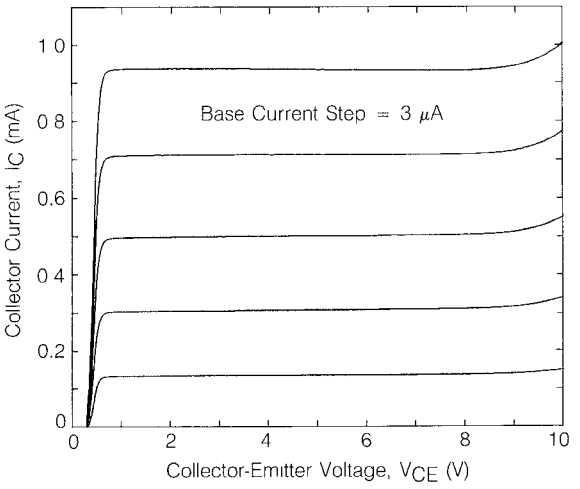


Fig. 5. Common-emitter collector current (I_C) versus collector–emitter voltage (V_{CE}) transfer characteristic (3 μA base current step) of a typical 3×10 μm^2 emitter SABM HBT with the epitaxial structure of Fig. 3. DC current gain $\beta \approx 60$ at $I_C \approx 1$ mA; β is proportional to $IC^{0.15}$ from $J_C \approx 30$–3000 A/cm^2.

of discussion a 3×10 μm^2 emitter HBT is chosen. The following HBT dc and RF characteristics (representive of typical devices) which affect analog and microwave performance are addressed here.

A. dc Characteristics

For 3×10 μm^2 HBT's, the fabrication process demonstrates nearly ideal transistor common-emitter collector current (I_C) versus collector-emitter voltage (V_{CE}) transfer characteristics, as exemplified in Fig. 5. Some of the key characteristics for the same measured device are noted:

1) Device Turn-On Threshold and Matching: Device matching is important for dc-coupled differential pair type circuit designs, which include most high-speed analog and A/D conversion circuits. In particular V_{BE} mismatch will result in distortion and reduced gain in differential amplifiers and degraded signal-to-noise ratio in A/D converters. The HBT turn-on voltage V_{BE} is determined by a combination of material and device design parameters and is approximated by the expression

$$V_{BE} \approx E_{gB}/q + (kT/q)\ln(N_A W_B I_C / qD_n N_C N_V A) + RI_C \quad (1)$$

where E_{gB} is the energy gap of the base, N_A is the base doping concentration, W_B is the base thickness, I_C is the corresponding collector current, D_n is the minority-carrier diffusion coefficient, N_C and N_V are the respective conduction and valence band density of states, A is the emitter–base junction area, and R is the parasitic resistance. At low currents V_{BE} is controlled by the energy band gap of the base and the emitter area, and at high currents V_{BE} is essentially dominated by the emitter contact resistance. In general the value of V_{BE} required to achieve a given I_C is expected to be highly uniform and reproducible (average $V_{BE} \approx 1.40$ V at $I_C \approx 1$ mA), whereas GaAs FET thresholds are primarily determined by processing (implant profile and active channel recessing). The typical V_{BE} matching of a 3×10 μm^2 emitter HBT at $I_C = 1$ mA is < 2 mV between closely spaced devices and < 5 mV for wafer matching.

2) Collector–Emitter Voltage Offset: The collector–emitter voltage V_{CE} offset (V_{CESAT0}) ≈ 250 mV (Fig. 5) results from a combination of the different turn-on voltages of the base–emitter heterojunction and the collector–base homojunction, different junction areas, excess recombination currents in the collector space-charge region, and resistive voltage drops between the external base contact and the intrinsic device. While V_{CESAT0} can be reduced to zero by implementing modified growth structures and device designs, the benefit is minimal since the typical offsets ≈ 250 mV are inconsequential for nonsaturating circuit applications.

3) Transconductance: The transconductance g_m is important in achieving small input voltage swing circuit operation, low (common-collector) output impedance for fast charging of load capacitances, and high voltage gain. For the bipolar transistor g_m is given by the expression

$$1/g_m = dV_{BE}/dI_C \approx 1/g_{m0} + R_E + R_B/\beta, \qquad g_{m0} = qI_C/kT \quad (2)$$

where g_{m0} is the intrinsic transconductance. The associated parasitic terms are the emitter resistance $R_E \approx 5$–$10\ \Omega$ and $R_B/\beta \approx 2\ \Omega$, with R_E becoming important at the higher current densities. The 3×10 μm^2 single-emitter HBT can be driven as high as $I_C \approx 40$ mA, or $J_C > 1\times10^5$ A/cm^2 without suffering from high injection in the base and Kirk ("base push-out") effects, which lead to a g_m as high as 40 K mS/mm (emitter length). For GaAs HBT's high current g_m operation is enhanced by the high base doping and high electron velocity, which minimizes high injection and Kirk effects to which Si bipolars are more susceptible. However, the benefits of operating at high g_m will be limited by metal migration and HBT reliability issues.

4) Output Conductance and Early Voltage: High voltage gain and device linearity result from high output conductance g_o, given by

$$g_o = dI_C/dV_{CE} = I_C/V_A \quad (3)$$

where V_A is the Early voltage, given by the expression

$$V_A = I_C/(dI_C/dV_{CE}) = -W_B(dV_{CE}/dW_B) \quad (4)$$

which describes the dependence of g_o on base width (W_B) modulation by V_{CE}. The intercept of the extrapolated I_C–V_{CE} slope with the negative V_{CE} axis (constant V_{BE}) gives the Early voltage $V_A \approx 800$ V. The high V_A, about 10–20 times higher than for Si bipolars, results from the GaAs HBT's high base doping, which minimizes base width modulation effects.

5) Common-Emitter Current Gain: While the heterojunction emitter concept has facilitated significant speed improvements, the associated common-emitter current gains critical in analog circuits have been limited. The HBT common-emitter current gain expressions are given

by

$$\beta = I_C/I_B \quad \text{and} \quad \Delta\beta = \Delta I_C/\Delta I_B \tag{5}$$

where β is the dc current gain and $\Delta\beta$ is the differential (small-signal) current gain, which are identical if β is constant with I_C. While ideal GaAs/AlGaAs HBT's project maximum β's of several thousand, this parameter is controlled by a combination of wide band gap heterojunction suppression of hole injection, base doping profile, and recombination effects which are determined by epitaxial growth and processing effects. In the useful J_C region of ≈ 30 to 3000 A/cm^2, β roll-off is very small, with β proportional to $\approx J_C^{0.15-0.25}$. These characteristics are comparable to the InP/In(Al,Ga)As type HBT's which report low β roll-off with J_C attributed to the lower surface recombination velocity effects [28]. The β variation within a wafer is typically 20–30 percent and can be as high as 100 percent from lot to lot, most likely related to a combination of base dopant diffusion control at the emitter–base heterojunction and surface recombination control in the emitter–base depletion region. While $\beta = 40$–60 ($J_C \approx 3$ kA/cm^2) is typical for the HBT process, the same epitaxial profile often yields $\beta \approx 100$. The dc current gain β is a critical parameter which is generally traded off with high-frequency performance in both the epitaxial growth structure and device processing (Fig. 2). High base doping reduces base resistance but degrades β via increased hole injection effects.

6) Breakdown Voltages: The basic breakdown voltage characteristics involving the collector–base junction, the emitter–base junction, and the collector–emitter structure govern the HBT operating limits such as linearity and output power and are traded off for speed. For the baseline HBT, the breakdown voltages are as follows:

- Collector–base junction breakdown (emitter open), BV_{CBO}: High BV_{CBO} is desired for high device linearity and high power applications. The HBT $BV_{CBO} \approx 14-16$ V is governed by the collector doping and width since the base is highly doped. Thicker and lower doped collectors reduce the breakdown voltage (avalanche process) but increase the effective transit times.
- Emitter–base junction breakdown (collector open), BV_{EBO}: This junction, which controls current gain, is the most sensitive to reverse bias currents which can damage the device. High BV_{EBO} is required in only a few applications, such as in the input comparators of a wide voltage range flash A/D converter. $BV_{EBO} \approx 3$–4 V is governed by the emitter doping. The breakdown mechanism is a combination of avalanche and Zener tunneling processes.
- Collector–emitter breakdown, BV_{CEO}: $BV_{CEO} \approx 9$ V (Fig. 5) is governed by collector–base breakdown coupled with a feedback multiplication factor of the current gain when measured with the base driven by a current source. Driving the base with a voltage source or low impedance, which is typically true in most applications, will result in a breakdown of about 12 V.

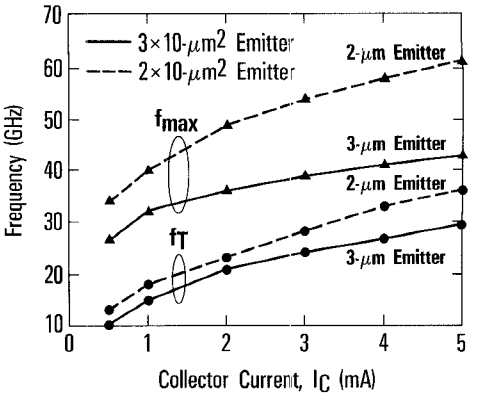


Fig. 6. On-wafer RF probe measured unity current gain cutoff frequency f_T and unity power gain f_{max} (derived from maximum available gain) for 3×10 μm^2 and 2×10 μm^2 emitter SABM HBT's (profile of Fig. 3).

B. High-Frequency Characteristics

The HBT figures of merit for frequency and speed performance [1], [29]–[31] are, first of all, the unity current gain cutoff frequency f_T, given by

$$1/2\pi f_T = t_{ec} = t_{ee} + t_b + t_c + t_{cc} \tag{6}$$

where t_{ec} is the total HBT input response delay time (or emitter to collector transit time), $t_{ee} = (kT/qI_C)C_{BE}$ is the emitter–base charging time, $t_b \approx (W_B^2/2D_n) + W_B/v_e$ is the base transit time including diffusion and drift type terms, t_c is the collector depletion layer transit time involving more complex velocity transport effects, and $t_{cc} = (kT/qI_C + R_E + R_C)C_{CB}$ is the collector charging time. Second, the maximum frequency of oscillation f_{max} (unity power gain) is approximated by

$$f_{max} \approx (f_T/8\pi R_B C_C)^{1/2} \tag{7}$$

and, third, the circuit switching time constant, t_s, is approximated by [31]

$$t_s \approx (5/2)R_B C_C + (R_B/R_L)t_b + (3C_C + C_L)R_L \tag{8}$$

where R_L and C_L are the circuit load resistance and capacitance, respectively.

The 3 μm SABM HBT has $f_T \approx 17$–28 GHz, $f_{max} \approx 30$–40 GHz (Fig. 6), and $t_s < 40$ ps for useful collector current densities $J_C \approx 3$–10 kA/cm^2 for a typical 3×10 μm^2 HBT. The HBT was designed for a higher f_{max} by optimizing the $R_B C_C$ charging time constant critical in microwave performance and digital circuit switching time. The effect of reducing the emitter width from 3 to 2 μm is to reduce the intrinsic collector–base capacitance and increase f_{max} by ~ 50 percent, as shown in Fig. 6. Parasitics become increasingly important with decreasing emitter width scaling. The f_T and f_{max} are derived from current gain (h_{21}) and maximum available gain (MAG) measurements, respectively, performed on-wafer from 1 to 26 GHz with higher values extrapolated (6 dB/octave). The lower f_T results from the high transit times associated with the relatively thick base (1400 Å) chosen to simplify processing

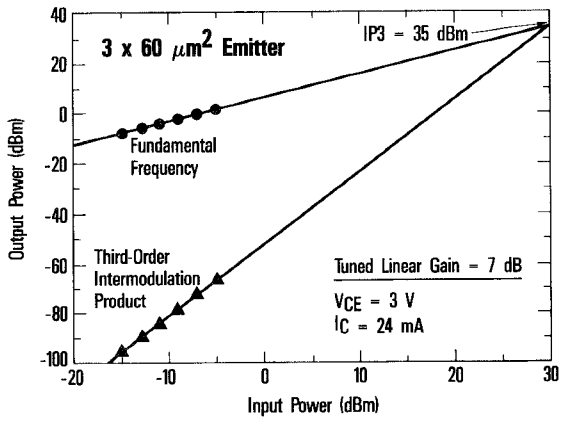


Fig. 7. The output tuned third-order intermodulation intercept point (IP3) of a 3×60 μm^2 emitter SABM HBT (profile of Fig. 3) at 12 GHz.

TABLE I
DEVICE TECHNOLOGY COMPARISON OF THIRD-ORDER INTERMODULATION INTERCEPT POINT (IP3) AT 12 GHz

12 GHz Performance							
TRW Device Structure	DC Power (mW)	Minimum Noise Figure (dB)	Gain (dB)	P_{out} 1 dB Comp. (dBm)	Power-Added Efficiency 1 dB Comp. (%)	IP3 (dBm)	Linearity Figure of Merit Ratio IP3 (mW) / DC Power (mW)
MESFET 0.5 x 300 μm^2 Gate	141 (3V, 47mA)	3.5	7.0	14.6	20	23.2	1.5
HEMT 0.25 x 200 μm^2 T-Gate	45 (3V, 15mA)	0.6	13.5	10.2	23	19.9	2.2
HBT 3 x 10 μm^2 Emitter	12 (3V, 4mA)	5.2	10.0	3.2	17	20.5	9.4
HBT 3 x 60 μm^2 Emitter	72 (3V, 24mA)	4.9	7.0	13.9	34	35.0	43.9

and reduce the base resistance and the thick collector (7000 Å) chosen to reduce the capacitance and increase the breakdown voltage. At low $J_C \approx 0.5$ to 3 kA/cm^2, where many digital and A/D devices are designed to operate, these f_T and $f_{max} \approx 10$–35 GHz are comparable to other reported HBT's with maximum f_T and f_{max} in the range of 100–200 GHz at $J_C \approx 10^5$ A/cm^2 using thinner bases (≈ 700 Å) and smaller emitter widths ≈ 1–2 μm [2], [22], [24].

C. Intrinsic Device Linearity

The HBT's high output impedance associated with the high Early voltage, high transconductance, and the slow variation of β with J_C can be used to achieve high linearity capabilities in device and circuit applications. An important application is linear amplifiers where minimizing harmonic distortion due to nonlinear mixing is critical. A critical measure of amplifier distortion is the two-tone third-order intermodulation intercept point (IP3), which is the extrapolated intersection of the third-order intermodulation product and the fundamental power output versus the input power (in dBm). The output tuned IP3 at 12 GHz of a 3×60 μm^2 HBT is shown in Fig. 7 [7]. Since the IP3 of an amplifier can be increased by using a larger device and increasing the dc power, a more useful figure of merit is the IP3/dc power ratio (in mW). For comparable devices and biases, the HBT is observed to have IP3/dc power ratio of 7–10 times higher than those of typical TRW MESFET and HEMT devices (Table I). Similar advantages are observed at 18 GHz using 3×20 μm^2 double-emitter HBT's with optimum biasing.

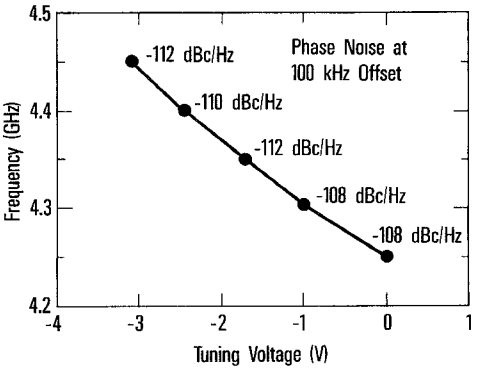


Fig. 8. Phase noise performance of a base-tuned, non-self-aligned version of the 3 μm emitter SABM HBT using a series $L-C$ resonant oscillator microstrip circuit.

D. Intrinsic Device Nonlinearity

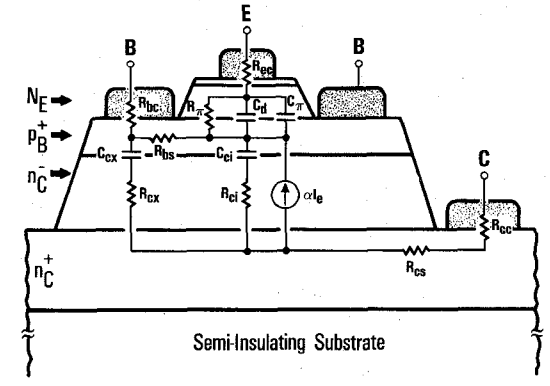
Just as the HBT has intrinsic characteristics that can be applied for high linearity applications, the HBT as a bipolar device has exponential output current–input voltage characteristic that can be used for nonlinear functions. These include limiting and logarithmic amplifiers and multiplier/mixers using differential HBT pairs.

E. Small Trapping Effects and Low $1/f$ (Phase) Noise Performance

The HBT's vertical current flow through well-shielded junctions leads to low trapping effects and low $1/f$ noise. Measured $1/f$ noise corner (white noise) frequency is comparable to Si bipolar transistors, in the order of tens to several hundred kHz. A direct effect is in the phase noise performance of the HBT in an oscillator circuit. Oscillator phase noise is dependent on the overall quality factor (Q) of the resonator (lower phase noise for higher Q) and the up-converted $1/f$ noise of the active devices. A series $L-C$ resonant circuit on a microstrip was used to evaluate the HBT related phase noise (Fig. 8). Phase noise of ≈ -110 dBc/Hz (100 kHz offset) at ≈ 4 GHz is observed for the non-self-aligned version of the 3×60 μm^2 HBT, which is similar to some of the best Si bipolar transistors evaluated in the same resonator (higher Q resonators are expected to give even lower phase noise with the HBT's). A 3×60 μm^2 SABM HBT yielded state-of-the-art phase noise of -82 dBc/Hz (100 kHz offset) at a tuned frequency of 37.7 GHz [7].

F. Device Models

Discrete HBT's are used to obtain both small-signal RF models for microwave applications and large-signal SPICE models for analog and digital circuit simulations; these models are rather conservative. The small-signal RF model derived from a physical HBT structure is shown in Fig. 9.



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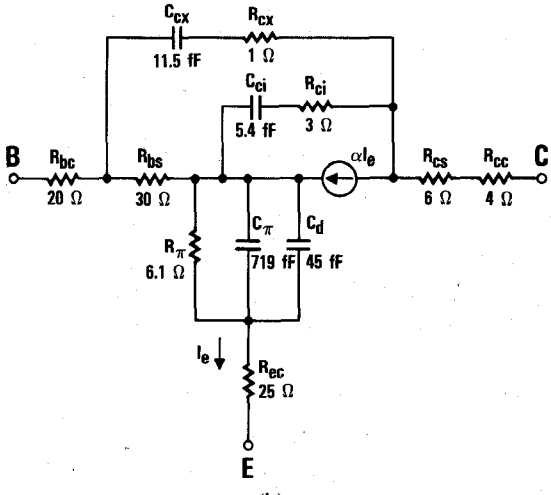


(b)

Fig. 9. (a) Physical device model of the 3×10 μm^2 emitter SABM HBT (profile of Fig. 3). (b) Corresponding small-signal lumped parameter RF model used to design microwave circuits.

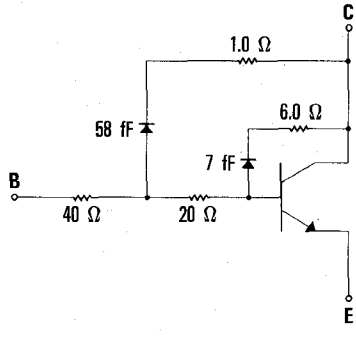


Fig. 10. HSPICE transistor model for the 3×10 μm^2 emitter SABM HBT (profile of Fig. 3) used to simulate analog, digital, A/D conversion, and multifunctional circuit performance. Conservative HSPICE parameters include dc current $\beta = 50$, forward transit time $t_F = 6$ ps, and Early voltage $V_A = 500$ V.

In the 3 μm SABM HBT the dominant parasitics are the base resistance and the external collector–base capacitance. Excellent fit to measured S parameters is achieved. A large-signal SPICE model derived from dc and RF measurements is shown in Fig. 10. Both analog and digital type circuits are simulated predicting actual operating bias and performance to within 10 percent.

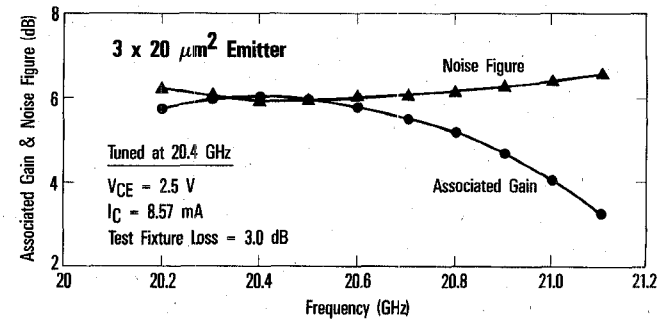


Fig. 11. Associated gain and noise figure of the 3×20 μm^2 emitter SABM HBT (profile of Fig. 3) amplifier at 20 GHz ($V_{CE} = 2.5$ V). The corresponding peak efficiency is 26 percent at 8.5 dBm output power and IP3 is 20 dBm.

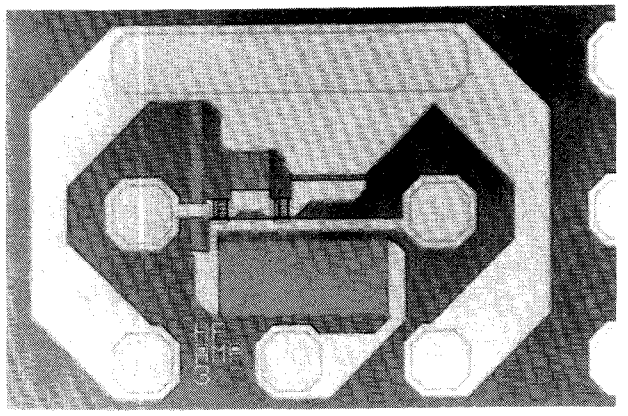
IV. HBT Device and Integrated Circuit Applications

The same 3 μm emitter SABM HBT device and IC process have been used to demonstrate important analog and microwave as well as digital and A/D conversion capabilities with the potential to achieve complex combined functions on the same monolithic chip. These functional demonstrations establish advantages over competitive approaches and are precursors to the development of specific devices and circuits for insertion into systems hardware. The TRW GaAs HBT development focuses on the next generation of system functions including communications (microwave, optical), electronic warfare (EW), and seekers. A key electronic subsystem required is the receiver, which is configured in various forms depending on the application, such as communications or EW. Advanced receivers currently under investigation are applying digital and wide-band techniques which require analog/microwave, digital, and A/D conversion functions. The impact of the 3 μm SABM HBT device/IC technology on such applications is presented through key examples of analog, microwave, and combined microwave/digital functions.

A. Analog and Microwave Applications

HBT's are ideal for linear, nonlinear, wide-dynamic-range, and low-phase-noise functions in receivers. The applications described here focus on small-signal, as opposed to power, at fundamental frequencies as high as 20 GHz (Fig. 11). Moderate power device development is in progress for phased-array applications. Analog and microwave functions involve discrete transistors and SSI–MSI complexity circuits whose yield and cost are expected to be competitive with high-performance Si bipolar technologies in a manufacturing environment.

1) Linear Functions: The HBT's combination of high intrinsic gain, high speed, and freedom from trapping effects makes it attractive for fixed-gain wide-band amplifiers important in communications and instrumentation. A hybrid four-link distributed amplifier using 3×10 μm^2 HBT's has been developed which has 10 dB flat gain to 9 GHz while requiring < 75 mW [32]. MMIC versions are currently under development. A similar wide-band perfor-



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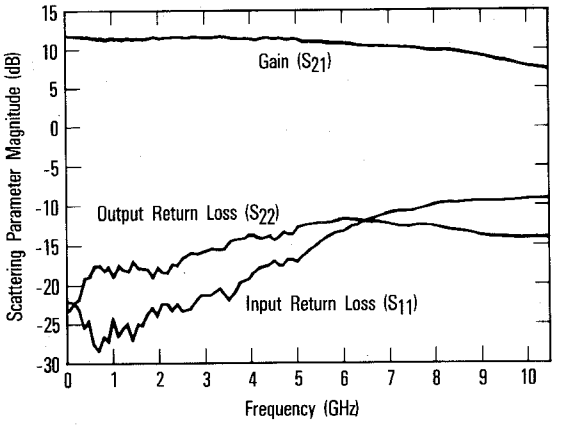
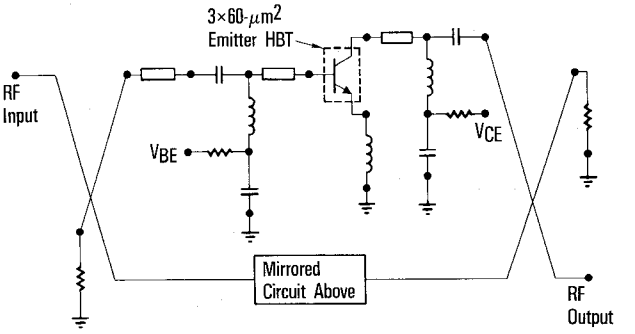


(b)

Fig. 12. GaAs HBT dc–10 GHz (3 dB) fixed gain monolithic Darlington-coupled feedback amplifier. (a) Fabricated on-wafer RF probe circuit (two HBT's, five resistors; chip size: 0.5×0.7 mm^2). (b) Measured (on-wafer) scattering parameters versus frequency, demonstrating flat 11 dB gain (±0.5 dB) from dc to 6 GHz. Input/output *VSWR*'s are $< 2.0:1$ over the 10 GHz bandwidth.



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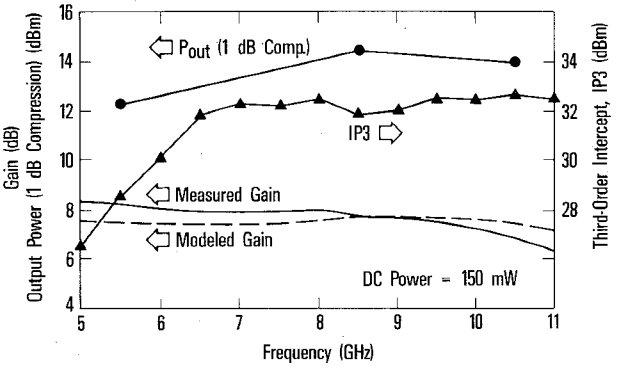


(b)

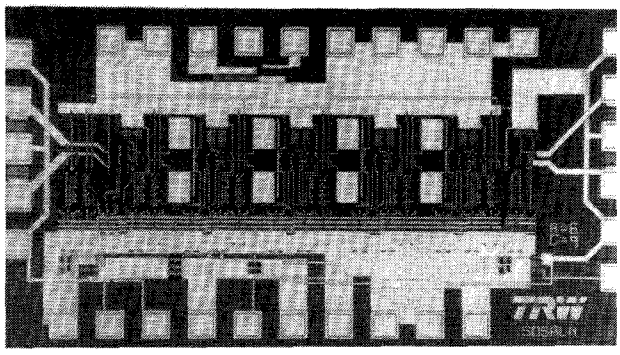
Fig. 13. GaAs HBT 5–11 GHz hybrid balanced amplifier designed for high linearity and low dc power. (a) Circuit design. (b) Measured gain, output power, and IP3.

mance has been realized using a very simple monolithic Darlington-coupled feedback amplifier design using two quad 3×10 μm^2 emitter HBT's and no input/output matching (Fig. 12). This amplifier has 11 ± 0.5 dB gain from dc to 6 GHz (10 GHz, -3 dB roll-off) with 480 mW dc power [33], demonstrating state-of-the-art performance in comparison with advanced bipolar [34] and MESFET approaches.

In multifrequency receiver environments, where harmonic distortion must be minimized, amplifier designs focus on high linearity. The measure of linearity is the intercept point of the fundamental frequency output with the intermodulation product, particularly the third-order IP3, as discussed earlier in Section III. The HBT's have high IP3 per input dc power, which is critical in space payload applications. Discrete HBT's have been used to develop a state-of-the-art, 5–11 GHz wide-band high-IP3 amplifier (Fig. 13) for use as the output stage to a HEMT input amplifier. The hybrid balanced amplifier has an IP3 of ≈ 33 dBm with 150 mW dc power, yielding an IP3 (mW)/dc power (mW) figure-of-merit ratio of 10.6 [32], which is a factor of 2–3 better than MESFET's and HEMT's. MMIC versions are currently in development.

Another example of the capability of the HBT is not only in the high-frequency area but also in low-frequency video applications, where GaAs MESFET's are limited due to trapping and hysteresis effects. The GaAs HBT advantages over Si bipolar are the high linearity (Early voltage) and the potential to integrate this type of lower frequency function with high-frequency digital and A/D functions required in advanced phase-locked loop synthesizers for future receivers. An ultralinear video amplifier (120 MHz, -3 dB bandwidth) developed for an HBT-based phase-locked loop synthesizer [35] yielded 12 dB gain (0.3 dB flatness), -85 dBc harmonic distortion, and $+40$ dBm IP3 in a 12.5 MHz bandwidth. For a 10 MHz input, the second harmonic is -82 dBc, and a third harmonic is -79 dBc. The harmonic distortion performance of this video amplifier exceeds some of the best Si bipolar versions by >10 dB. Also, a monolithic operational amplifier designed to achieve a proportional-to-absolute-temperature (PTAT) current source function has been demonstrated [36]. The monolithic op amp has an open-loop gain of 1 K, unity gain bandwidth of 50 MHz, 20 mW power consumption, and operates from a single -5 or $+5$ V supply.

2) Nonlinear Functions: Logarithmic amplifiers are critical components in radar, electronic warfare (EW), sonar/ultrasound, and instrumentation applications requiring the compression of wide-dynamic-range signals,



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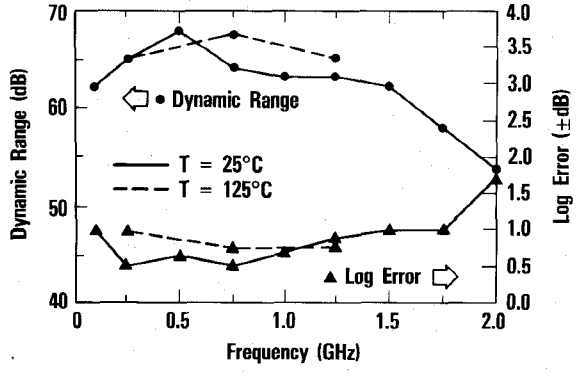

(b)

Fig. 14. GaAs HBT monolithic successive-detection logarithmic IF amplifier with $<1/5$ power consumption and $<1/20$ size of comparable performance Si-based hybrid log amps. (a) Fabricated five-stage circuit (129 HBT's; chip size: 1.2×2.4 mm^2). (b) Measured (on-wafer) dynamic range and log error.

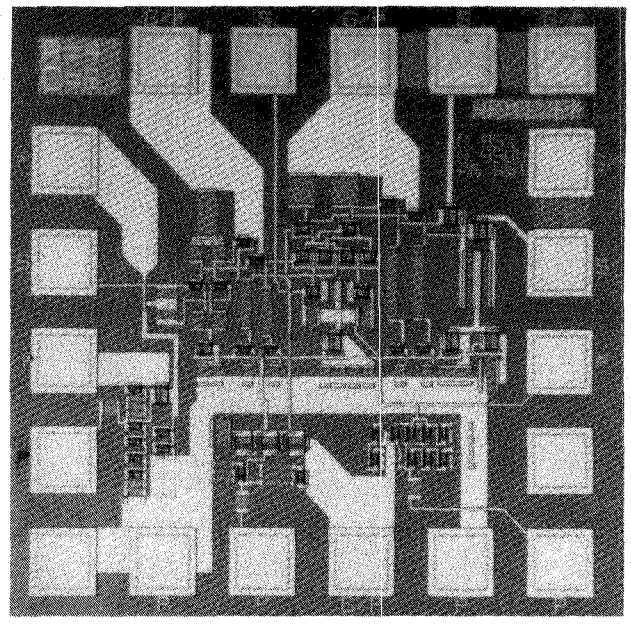

Fig. 15. GaAs HBT four-quadrant (Gilbert cell) multiplier/mixer fabricated circuit (46 HBT's; chip size: 0.95×0.95 mm^2). Measured (on-wafer) performance includes 10 dB gain, >5 GHz RF output, <-55 dBc for 2LO–2IF spur, and <-95 dBc for 2LO–6IF spur.

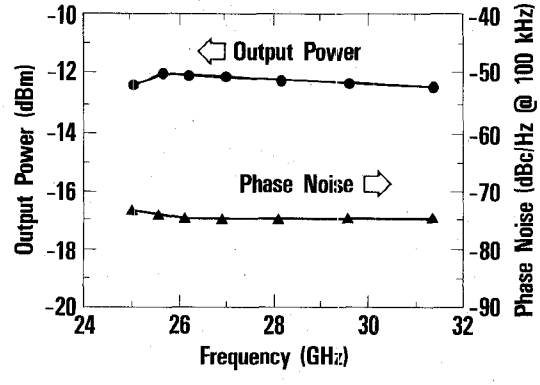

Fig. 16. Output power and phase noise for a GaAs HBT 25–32 GHz hybrid push–push voltage-controlled oscillator based on a series-resonant L–C topology.

beyond the usefulness of linear amplification (e.g. automatic gain control). Typical applications include phased-array antennas, monopulse direction finding, target identification, electronic countermeasures (ECM), sonar signal amplification, ultrasound scanning, and power measurement. Second-generation HBT monolithic log IF amplifiers (Fig. 14) with 60 dB dynamic range (±1 dB log error) over 0.5–1.5 GHz have been demonstrated [12]. The excellent differential amplifier performance, combined with low delay–power product and semi-insulating substrate for high isolation, results in single-chip 65 dB dynamic range successive-detection log IF amplifiers (SDLA) with 1/5 the power consumption (380 mW), 1/20 the size, and twice the bandwidth of commercial Si-based hybrid log amps. Operation up to 125°C demonstrates the intrinsic capability of the GaAs HBT to satisfy military temperature standards. A monolithic GaAs MESFET SDLA log amp has been reported [37] with similar performance advantage over the Si hybrid, but with twice the power consumption and log error of the HBT circuit.

The exponential output current–input voltage transfer function of the HBT also allows high-performance mixer functions to be realized. A four-quadrant (Gilbert cell) linear multiplier has been developed (Fig. 15) for use as a mixer to achieve spectrally clean output signal [38]. The intrinsic gain of the differential cross-coupled amplifiers permits conversion gain while the differential topology minimizes input/output matching, resulting in a compact chip. The Gilbert-cell mixer chip has >10 dB conversion gain at >5 GHz RF output. Initial measured spurious response includes <-55 dBc for 2LO–2IF spur and <-95 dBc for 2LO–6IF spur. These capabilities offer attractive alternatives to MESFET mixers.

3) Oscillators: Oscillators are one of the key applications for the HBT because of the combined high-frequency and low-phase-noise capabilities. Discrete 3×60 μm^2 emitter HBT's have been used to demonstrate a tuned oscillation frequency of 37.7 GHz with -82 dBc/Hz (100 kHz offset). These devices were configured into a hybrid push–push, frequency-doubling voltage-controlled oscillator (VCO) for frequency tuning over 25–32 GHz with state-of-the art phase noise performance (Fig. 16) [7]. The push–push oscillation scheme is widely used to generate

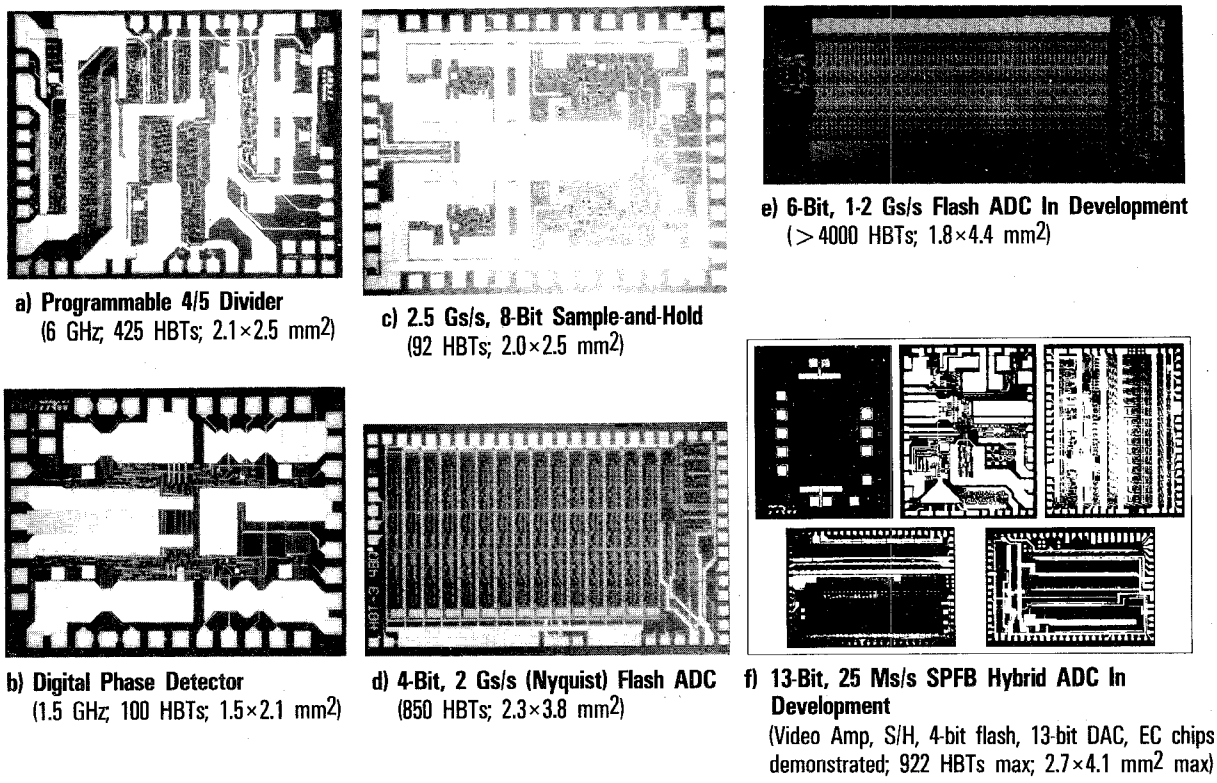

Fig. 17. GaAs HBT digital and A/D conversion functions demonstrated and in development using the same analog/microwave fabrication process including (a) programmable 4/5 divider, (b) digital phase detector, (c) sample-and-hold amplifier, (d) 4-bit flash A/D converter, (e) LSI 6-bit flash A/D converter (in development), and (f) demonstrated component chips for a 13-bit hybrid series-parallel feedback (SPFB) A/D converter.

signals beyond the frequency range where the active device is limited in gain [39]. This particular HBT VCO is part of an advanced communications receiver development effort.

B. Monolithically Combined Microwave/Digital Applications

The same 3 μm emitter SABM HBT IC process used to achieve dc to 20 GHz analog and microwave capabilities has been used to demonstrate the advanced digital and analog/digital conversion circuit functions shown in Fig. 17. These capabilities make the HBT technology ideal for single-chip A/D conversion and digital processing of analog/microwave signals. Actually, simultaneous analog and digital functions (operating in the 1–3 GHz regime) are already present in the A/D conversion circuits. Combined microwave, high-speed digital, and A/D conversion functions with frequencies >10 GHz are possible since dc–10 GHz wide-band amplifiers and >10 GHz dividers (with $\beta \approx 50$–100) have been demonstrated on the same wafer. An example of a multifunctional integration is a 7 GHz amplifier/digital divide-by-4 developed for synthesizer applications. A single chip is used to amplify a microwave signal (as low as −25 dBm) to a level suitable for digital division up to 7 GHz (on-wafer test limited). Another example is a digitally controlled switched gain/attenuator amplifier, shown in Fig. 18 [13], designed for application to EW receivers. Five-bit binary control (TTL compatible) is used to switch combinations of successive gain and attenuation stage with full monotonicity. Its performance includes a 62 dB dynamic range (+31 to −31 dB, in 2 dB increments) from dc to 2.5 GHz, less than 1.6 dB RMS gain error across the band, and less than 1.3 W power consumption. This frequency regime is less attractive for GaAs MESFET applications due to trapping effects, and the HBT's advantage over Si bipolar is the higher gain–bandwidth product and the potential for monolithic integration with higher frequency microwave functions. More complex applications could include combinations of RF mixers, log amplifiers, A/D converters, and digital control and high-speed logic. Monolithic integration of VCO's may be limited by isolation and spur requirements.

V. Technology Insertion Qualification

The insertion of the 3 μm SABM HBT technology into systems requires basic qualification in temperature performance, reliability, and radiation hardness. This section presents initial qualification work performed on this process. Although more thorough statistical studies are required, the initial work shows no intrinsic limitations for even the most stringent space qualification (S-class) applications.

A. High-Temperature Performance

The 3 μm SABM HBT has demonstrated device and circuit operational capability up to 125°C (mil standard). The key device parameters that need to be compensated

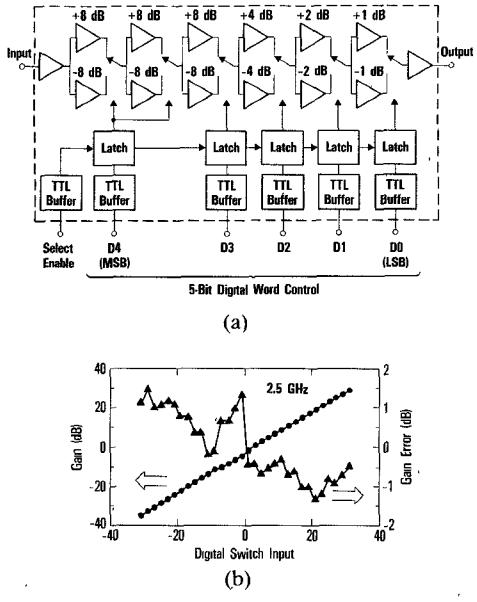

Fig. 18. DC–2.5 GHz, 5-bit digitally controlled switched gain/attenuator amplifier with 62 dB dynamic range in 2 dB increments demonstrating monolithically combined microwave/digital function using the 3 μm emitter SABM HBT IC process. (a) Block diagram; D4-D0 are the input digital word bits (TTL compatible); fabricated circuit (377 HBT's; chip size: 1.7×2.2 mm^2). (b) Measured (on-wafer) gain and error versus input digital word.

for temperature include the intrinsic transconductance g_{m0} and current gain β. The intrinsic g_{m0} is just qI_C/kT while β and V_{BE} have negative temperature coefficients of ≈ -0.4 percent/°C and -1.5 mV/°C, respectively. These parameters are compensated for using circuit design techniques. Examples of intrinsic high-temperature capabilities of the HBT in circuit operation are given by the SDLA log IF amplifier (Fig. 14(b)) and the digitally switched gain/attenuator (Fig. 18) discussed earlier, which operate to nominal specifications up to 125°C.

B. Reliability

Reliability qualification has been initiated for the 3 μm SABM HBT IC process. The procedure follows the work in progress for the GaAs MESFET MMIC's that are being developed for space applications. Stabilization bake, accelerated life testing, and step-stress testing are presently in progress. The initial stabilization bake is intended to stabilize the device parameters prior to accelerated aging and step-stress tests and to screen for infant mortality. The HBT's are subjected to 260°C for 120–160 hours in a nitrogen ambient where the dc parameters (β and emitter and base contact resistances) stabilize to less than 5 percent of the initial values. Accelerated life tests include aging at 260°C under dc bias. The step-stress testing at 220, 240, and 260°C is designed to extract the activation energy to determine the mean time to failure.

Initial accelerated life testing with small sample size (six HBT's) verifies HBT lifetime capability beyond 2000 hours at 260°C with <20 percent dc parameter degradation. The devices aged under nominal operating dc bias were periodically removed and tested for β, I_C ideality factor,

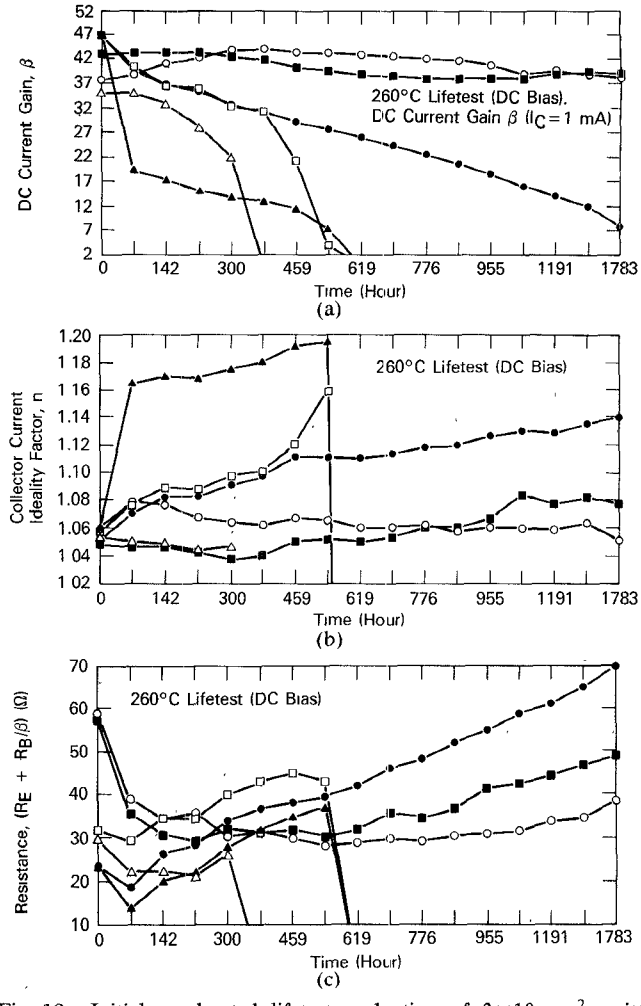

Fig. 19. Initial accelerated lifetest evaluation of 3×10 μm^2 emitter SABM HBT's at 260°C (under dc bias) after 120–160 hours stabilization bake. (a) β versus time. (b) I_C ideality factor n versus time. (c) Device resistance ($R_E + R_B/\beta$) versus time.

and contact resistances, as summarized in Fig. 19. The long-life devices show gradual parameter degradations which are consistent with one another. Scanning electron microscope diagnostics on devices that failed early did not show any obvious catastrophic failure such as bond wire lifting or metal burnout. The consistent device parameter degradation suggests failure related to the emitter–base space charge region, perhaps due to surface leakage and device shorting associated with contaminants or ohmic metal definition. Accelerated aging studies and step-stress tests with larger HBT sample size are currently in progress. Circuit reliability testing (log amplifiers and digital dividers) is also being performed.

C. Radiation Hardness

Semiconductor devices in space radiation (Van Allen belt) and nuclear explosion environments can suffer crystalline lattice displacement (defects) and ionization (generation of electron–hole pairs) effects. Radiation environments are generally classified into four different categories according to their sources: 1) total ionizing dose, 2) neutron, 3) dose rate, and 4) single-event upset (SEU) environ-

TABLE II
RADIATION HARDNESS COMPARISON OF DEVICE TECHNOLOGIES

ENVIRONMENT / TECHNOLOGY	Electrical			Radiation					
						Dose Rate [Rad(Si or GaAs)/s]			
						Upset			Burnout
	Speed	Power Dissipation	Integration Level	Total Dose [Rad(Si) or Rad(GaAs)]	Neutron [n(1-MeV)/cm^2]	Digital	Analog	Latch-Up	
Silicon									
CMOS									
Non-Hardened	Low	Low	VLSI	10^3–10^4	10^{13}	10^6–10^7		10^7–10^9	10^{10}–10^{12}
Hardened				10^5–10^6	$>10^{14}$	10^8–10^9		$>10^{12}$	$>10^{12}$
SOS/SOI				10^5–10^6	$>10^{14}$	10^{10}–10^{11}		No	$>10^{12}$
Bipolar									
Linear	Medium	High	VLSI	10^4–10^5	10^{12}–10^{13}			10^7–10^9	10^{10}–10^{12}
Digital				$>10^6$	10^{13}–10^{14}	10^6–10^7	$<10^6$	10^7–10^9	
Digital/ROX				10^4–10^5					
Digital/Hardened				$>10^6$	10^{13}–10^{14}	10^7–10^8		$>10^{12}$	$>10^{12}$
GaAs								Backgating	
MESFET/HEMT									
RF	High	Medium	LSI	$>10^8$	$>10^{14}$		10^9–10^{10}	Yes*	10^{10}–10^{12}
Digital				$>10^8$	$>10^{15}$	10^{10}–10^{11}		Yes*	
JFET	Medium	High	LSI	$>10^8$	$>10^{15}$	10^{10}–10^{11}		Yes*	10^{13}
HBT									
RF	**High**	**High**	**MSI-LSI**	**$>10^8$**	**$>10^{14}$**		**10^9–10^{10}**	**No***	
Digital				**$>10^8$**	**$>10^{15}$**	**10^{10}–10^{11}**		**No***	

*For All Dose Rates

ments. The displacement alters the device performance by reduction of minority carrier lifetime, majority carrier removal (trapping and compensation), and mobility degradation. The ionization interaction in a low-dose-rate environment causes gradual charging of dielectric regions while a high-dose-rate environment causes transient photocurrents. Initial investigation with the 3 μm SABM HBT shows excellent radiation hardness compared to other technologies in total dose, neutron, and dose rate (Table II). The initial tests performed on a limited number of transistors [21] show radiation hardness significantly greater than Si and comparable to that of MESFET's with the exception of dose rate in which the HBT's are free from the long-term transients which typically plague GaAs MESFET's. SEU was not investigated due to a lack of a convenient MSI–LSI digital test vehicle at this time.

In total dose testing a Co^{60} source provides gamma ray radiation which generates Compton electrons, accumulated over a long term. The damage is considered permanent. The total dose environment appears to be the least harmful to the HBT with β degrading ≈ 7 percent in the dose range up to 467 Mrad(GaAs), most likely due to displacement damage. The high total dose tolerance may be due to the high density of electron and hole charge trap centers in the silicon nitride passivation and the intrinsically high GaAs surface state density.

A more sensitive radiation effect in GaAs HBTs appears to be neutron damage showing β degradation of ≈ 20 percent at $\approx 1.3\times10^{14}$ n/cm^2. Gummel plots show that the ideality factor of emitter–base (E–B) junctions approaches 2 afte. neutron irradiation, suggesting that the generation of recombination centers associated with that junction is important. To simulate the ideality factor reduction using physical device modeling (modified SEDAN), the width of the E–B space charge region where the recombination is assumed had to be increased from 10 to 30 Å. No ideality factor degradation was observed for the collector–base junction. A 20 percent reduction in β will seriously affect some analog circuit applications while in digital and microwave applications, β reductions of up to 50 percent are acceptable. Data extrapolation indicates digital IC neutron hardness to be an order of magnitude greater than for analog circuits. The neutron data can be correlated with the total dose data by establishing the damage equivalence between Co^{60} gamma rays. A 467 Mrad damage is equivalent to $2.7-5.3\times10^{13}$ n(1 MeV Equiv.)/cm^2. By comparing β reduction at the corresponding levels in each radiation environment, similar results are obtained.

Dose rate tests were performed using flash X-ray pulses ≈ 22 ns wide. The HBT transient collector current recovery time is on the order of a few microseconds, as opposed to GaAs MESFET's with longer recovery times ($\approx$ milliseconds) due to active channel–substrate interface trapping effects. The lack of long-term transients in HBT's is due to the vertical structure with active junctions isolated from surfaces and substrate interfaces. In particular the n^+ collector contact layer tends to screen out bias resulting from trapped charge in the semi-insulating substrate. Also, since HBT IC's do not use p-n junction isolation, latchup is not possible. Dose rate effects are important since they may upset circuit functions and may cause burnout of junctions or interconnects associated with high or multiplied photocurrents.

Another transient radiation effect is the single-event upset, or SEU. High-energy galactic particles, protons, and solar flare ions are the main source of SEU in space while alpha particles (helium nuclei) from minute traces of radioisotopes in ceramic chip packages can cause the same effect in nonspace environments. Excess carriers generated by these heavily ionizing particles incident on sensitive junctions are collected to create subnanosecond current pulses. Circuit upsets can result from a single particle confined to a single node. In some cases single-event currents are regeneratively amplified in a device to cause burnout. SEU testing for GaAs HBT IC's is currently being planned.

VI. Summary and Conclusions

The GaAs/AlGaAs N-p-n HBT device and integrated circuit technology offers key advantages over the most competitive advanced Si bipolar and III–V compound field-effect transistor (GaAs MESFET/HEMT) approaches in focused high-performance analog and microwave applications. This was exemplified through discussions based primarily on TRW's first generation GaAs HBT IC technology currently being transferred to a pilot production facility in preparation for application to communications, electronic warfare, and missile seeker systems. Device and IC fabrication process, basic HBT dc and RF performance, examples of device and IC applications, and technology qualification work were presented addressing important technology issues and impact.

Although the GaAs HBT fabrication technology is evolving with more advanced material and device structures, a relaxed 3 μm emitter self-aligned base ohmic metal (SABM) process with simplified MBE growth structure still offers many advantages over alternative current and projected device technologies. The 3 μm SABM HBT's have simultaneous $f_t, f_{\max} \approx 20$–40 GHz and dc current gain $\beta \approx 50$–100 at useful collector current densities $J_C \approx 3$–10 kA/cm^2 and Early voltage $V_A \approx 500$–1000 V. Using nonsaturating HBT operation, versatile dc–20 GHz analog and microwave as well as 3–6 Gbit/s digital and 2–3 Gs/s A/D conversion capabilities are demonstrated with the same 3 μm SABM HBT process which also facilitates monolithic multifunctional capabilities. Key improvements are realized over Si bipolar and GaAs-related FET approaches in operational frequency, power consumption, gain–bandwidth product, harmonic distortion, $1/f$ noise, and size reduction. Technology insertion qualification included initial verification of high-temperature operation (125°C), reliability (> 2000 hour lifetime at 260°C), and radiation hardness, with the latter being significantly better than Si bipolar and comparable to the GaAs MESFET.

The GaAs HBT is emerging as a technology which will complement the GaAs FET's and Si bipolar to achieve more efficient system functions. Its future competitiveness in niche applications as well as its expanding role will be ensured through the significant growth potential in materials, processing, and design techniques.

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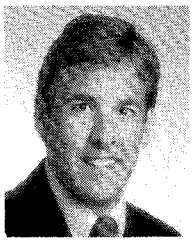

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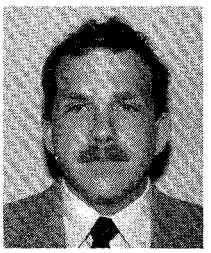

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